Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a capacitor having first and second electrodes;

an inverter whose input terminal is connected to the first electrode; and

a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of the capacitor during a reset period,

wherein the digital signal is input to the second electrode of the capacitor ~~means~~ during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

2. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a capacitor having first and second electrodes;

an inverter whose input terminal is connected to the first electrode;

a first switch connected between the input terminal and an output terminal of the inverter; and

second and third switches connected to the second electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor during a reset period,

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor ~~means~~ during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

3-6. (Canceled)

7. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a first capacitor having first and second electrodes;

a second capacitor having third and fourth electrodes;

an inverter whose input terminal is connected to the first electrode and the third electrode; and

a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of the first capacitor and a second potential is input to the fourth electrode of the second capacitor during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor ~~means~~ and to the fourth electrode of the second capacitor during a sampling period after the reset period.

8. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a first capacitor having first and second electrodes;

a second capacitor having third and fourth electrodes;

an inverter whose input terminal is connected to the first electrode and the third electrode;

a first switch connected between the input terminal and an output terminal of the inverter;

second and third switches connected to the second electrode; and

fourth and fifth switches connected to the fourth electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the first capacitor while the fourth switch is turned ON to input a second potential to the fourth electrode of the second capacitor ~~means~~ during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the first capacitor ~~means~~ while the fifth switch is turned ON to input the digital signal to the

fourth electrode of the second capacitor during a sampling period after the reset period.

9-10. (Canceled)

11. (Previously Presented) The data latch circuit according to claim 7, wherein the first potential is a potential of 1 or 0 as the digital signal.

12. (Previously Presented) The data latch circuit according to claim 8, wherein the first potential is a potential of 1 or 0 as the digital signal.

13. (Canceled)

14. (Previously Presented) The data latch circuit according to claim 1, wherein the reset period is determined with a first sampling pulse from a first delayed flip-flop while the sampling period is determined with a second sampling pulse from a second delayed flip-flop.

15. (Previously Presented) The data latch circuit according to claim 2, wherein the reset period is determined with a first sampling pulse from a first delayed flip-flop while the sampling period is determined with a second sampling pulse from a second delayed flip-flop.

16-19. (Canceled)

20. (Previously Presented) The data latch circuit according to claim 7, wherein the reset period is determined with a first sampling pulse from a first delayed flip-flop-while the sampling period is determined with a second sampling pulse from a second delayed flip-flop.

21. (Previously Presented) The data latch circuit according to claim 8, wherein the reset period is determined with a first sampling pulse from a first delayed flip-flop-while the sampling

period is determined with a second sampling pulse from a second delayed flip-flop.

22-23. (Canceled)

24. (Previously Presented) The data latch circuit according to claim 1, wherein an amplitude between the high level and the low level of the digital signal is smaller than an amplitude of an output of the inverter.

25. (Previously Presented) The data latch circuit according to claim 2, wherein an amplitude between the high level and the low level of the digital signal is smaller than an amplitude of an output of the inverter.

26-29. (Canceled)

30. (Previously Presented) The data latch circuit according to claim 7, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

31. (Previously Presented) The data latch circuit according to claim 8, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

32-36. (Canceled)

37. (Previously Presented) The data latch circuit according to claim 1, wherein the data latch circuit is formed by using thin film transistors.

38. (Previously Presented) The data latch circuit according to claim 2, wherein the data

latch circuit is formed by using thin film transistors.

39-42. (Canceled)

43. (Previously Presented) The data latch circuit according to claim 7, wherein the data latch circuit is formed by using thin film transistors.

44. (Previously Presented) The data latch circuit according to claim 8, wherein the data latch circuit is formed by using thin film transistors.

45-46. (Canceled)

47. (Previously Presented) An electronic device having the data latch circuit according to claim 1, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

48. (Previously Presented) An electronic device having the data latch circuit according to claim 2, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

49-52. (Canceled)

53. (Previously Presented) An electronic device having the data latch circuit according to claim 7, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

54. (Previously Presented) An electronic device having the data latch circuit according to claim 8, wherein the electronic device is selected from the group consisting of a display, a mobile

computer, a game machine, a mobile phone, a navigation system, and a camera.

55-56. (Canceled)

57. (Previously Presented) A semiconductor device comprising:

a data latch circuit which samples a digital signal,

wherein the data latch circuit comprises a capacitor having first and second electrodes, an inverter whose input terminal is connected to the first electrode, and a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of the capacitor during a reset period,

wherein the digital signal is input to the second electrode of the capacitor during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

58. (Previously Presented) The semiconductor device according to claim 57, wherein an amplitude between the high level and the low level of the digital signal is smaller than an amplitude of an output of the inverter.

59. (Previously Presented) The semiconductor device according to claim 57, wherein the data latch circuit is formed by using thin film transistors.

60. (Previously Presented) An electronic device having the semiconductor device according to claim 57, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

61. (Previously Presented) A semiconductor device comprising:

a data latch circuit which samples a digital signal,

wherein the data latch circuit comprises a capacitor having first and second electrodes, an inverter whose input terminal is connected to the first electrode, a first switch connected between the input terminal and an output terminal of the inverter, and second and third switches connected to the second electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor during a reset period,

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

62. (Previously Presented) The semiconductor device according to claim 61, wherein an amplitude between the high level and the low level of the digital signal is smaller than an amplitude of an output of the inverter.

63. (Previously Presented) The semiconductor device according to claim 61, wherein the data latch circuit is formed by using thin film transistors.

64. (Previously Presented) An electronic device having the semiconductor device according to claim 61, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

65. (Previously Presented) A semiconductor device comprising:

a data latch circuit which samples a digital signal,

wherein the data latch circuit comprises a first capacitor having first and second electrodes, a second capacitor having third and fourth electrodes, an inverter whose input terminal is connected to the first electrode and the third electrode, and a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of

the first capacitor and a second potential is input to the fourth electrode of the second capacitor during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor and to the fourth electrode of the second capacitor during a sampling period after the reset period.

66. (Previously Presented) The semiconductor device according to claim 65, wherein the first potential is a potential of 1 or 0 as the digital signal.

67. (Previously Presented) The semiconductor device according to claim 65, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

68. (Previously Presented) The semiconductor device according to claim 65, wherein the data latch circuit is formed by using thin film transistors.

69. (Previously Presented) An electronic device having the semiconductor device according to claim 65, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

70. (Previously Presented) A semiconductor device comprising:

a data latch circuit which samples a digital signal,

wherein the data latch circuit comprises, a first capacitor having first and second electrodes, a second capacitor having third and fourth electrodes, an inverter whose input terminal is connected to the first electrode and the third electrode, a first switch connected between the input terminal and an output terminal of the inverter, second and third switches connected to the second electrode, and fourth and fifth switches connected to the fourth electrode,

wherein the first switch and the second switch are turned ON to input a first potential to

the second electrode of the first capacitor while the fourth switch is turned ON to input a second potential to the fourth electrode of the second capacitor during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the first capacitor while the fifth switch is turned ON to input the digital signal to the fourth electrode of the second capacitor during a sampling period after the reset period.

71. (Previously Presented) The semiconductor device according to, claim 70, wherein the first potential is a potential of 1 or 0 as the digital signal.

72. (Previously Presented) The semiconductor device according to claim 70, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

73. (Previously Presented) The semiconductor device according to claim 70, wherein the data latch circuit is formed by using thin film transistors.

74. (Previously Presented) An electronic device having the semiconductor device according to claim 70, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

75. (Previously Presented) A semiconductor device comprising:

a shift register having at least a first circuit and a second circuit;

at least first and second data latch circuits which sample a digital signal,

wherein the at least first and second data latch circuits are connected to the shift register,

wherein each of the first and the second data latch circuits comprises a capacitor having first and second electrodes, an inverter whose input terminal is connected to the first electrode; and a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of

the capacitor during a reset period,

wherein the digital signal is input to the second electrode of the capacitor during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

76. (Previously Presented) The semiconductor device according to claim 75, wherein the reset period is determined with a first sampling pulse from the first circuit of the shift register while the sampling period is determined with a second sampling pulse from the second circuit of the shift register.

77. (Previously Presented) The semiconductor device according to claim 75, wherein an amplitude between the high level and the low level of the digital signal is smaller than amplitude of an output of the inverter.

78. (Previously Presented) The semiconductor device according to claim 75, wherein the first and the second data latch circuits are formed by using thin film transistors.

79. (Previously Presented) An electronic device having the semiconductor device according to claim 75, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

80. (Previously Presented) A semiconductor device comprising:

a shift register having at least a first circuit and a second circuit;

at least first and second data latch circuits which sample a digital signal,

wherein the at least first and second data latch circuits are connected to the shift register,

wherein each of the first and the second data latch circuits comprises a capacitor having first and second electrodes, an inverter whose input terminal is connected to the first electrode, a first switch connected between the input terminal and an output terminal of the inverter, and

second and third switches connected to the second electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor during a reset period,

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor during a sampling period after the reset period, and

wherein the first potential is one of a high level and a low level of the digital signal.

81. (Previously Presented) The semiconductor device according to claim 80, wherein the reset period is determined with a first sampling pulse from the first circuit of the shift register while the sampling period is determined with a second sampling pulse from the second circuit of the shift register.

82. (Previously Presented) The semiconductor device according to claim 80, wherein an amplitude between the high level and the low level of the digital signal is smaller than an amplitude of an output of the inverter.

83. (Previously Presented) The semiconductor device according to claim 80, wherein the first and the second data latch circuits are formed by using thin film transistors.

84. (Previously Presented) An electronic device having the semiconductor device according to claim 80, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

85. (Previously Presented) A semiconductor device comprising:

a shift register having at least a first circuit and a second circuit;

at least first and second data latch circuits which sample a digital signal,

wherein the at least first and second data latch circuits are connected to the shift register,

wherein each of the first and the second data latch circuits comprises a first capacitor

having first and second electrodes, a second capacitor having third and fourth electrodes, an inverter whose input terminal is connected to the first electrode and the third electrode, and a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON and a first potential is input to the second electrode of the first capacitor and a second potential is input to the fourth electrode of the second capacitor during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor and to the fourth electrode of the second capacitor during a sampling period after the reset period.

86. (Previously Presented) The semiconductor device according to claim 85, wherein the first potential is a potential of 1 or 0 as the digital signal.

87. (Previously Presented) The semiconductor device according to claim 85, wherein the reset period is determined with a first sampling pulse from the first circuit of the shift register while the sampling period is determined with a second sampling pulse from the second circuit of the shift register.

88. (Previously Presented) The semiconductor device according to claim 85, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

89. (Previously Presented) The semiconductor device according to claim 85, wherein the first and the second data latch circuits are formed by using thin film transistors.

90. (Previously Presented) An electronic device having the semiconductor device according to claim 85, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

91. (Previously Presented) A semiconductor device comprising:

a shift register having at least a first circuit and a second circuit

at least first and second data latch circuits which sample a digital signal,

wherein the at least first and second data latch circuits are connected to the shift register,

wherein each of the first and the second data latch circuits comprises a first capacitor having first and second electrodes, a second capacitor having third and fourth electrodes, an inverter whose input terminal is connected to the first electrode and the third electrode, a first switch connected between the input terminal and an output terminal of the inverter, second and third switches connected to the second electrode, and fourth and fifth switches connected to the fourth electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the first capacitor while the fourth switch is turned ON to input a second potential to the fourth electrode of the second capacitor during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the first capacitor while the fifth switch is turned ON to input the digital signal to the fourth electrode of the second capacitor during a sampling period after the reset period.

92. (Previously Presented) The semiconductor device according to claim 91, wherein the first potential is a potential of 1 or 0 as the digital signal.

93. (Previously Presented) The semiconductor device according to claim 91, wherein the reset period is determined with a first sampling pulse from the first circuit of the shift register while the sampling period is determined with a second sampling pulse from the second circuit of the shift register.

94. (Previously Presented) The semiconductor device according to claim 91, wherein an amplitude between the first potential and the second potential is smaller than an amplitude of an output of the inverter.

95. (Previously Presented) The semiconductor device according to claim 91, wherein the first and the second data latch circuits are formed by using thin film transistors.

96. (Previously Presented) An electronic device having the semiconductor device according to claim 91, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.